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Graphene Transistors via in Situ Voltage-Induced Reduction of Graphene-Oxide under Ambient Conditions

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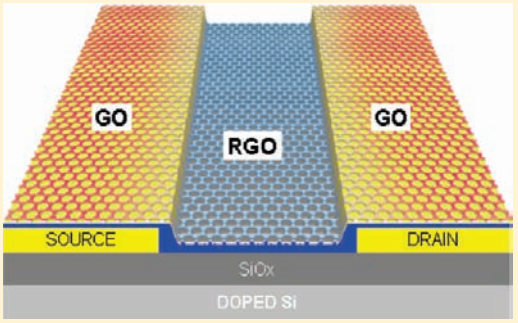
Supporting Information

ABSTRACT: Here, we describe a simple approach to fabricate graphene-based field-effect-transistors (FETs), starting from aqueous solutions of graphene-oxide (GO), processed entirely under ambient conditions. The process relies on the site-selective reduction of GO sheets deposited in between or on the surface of micro/nanoelectrodes. The same electrodes are first used for voltage-induced electrochemical GO reduction, and then as the source and drain contacts of FETs, allowing for the straightforward production and characterization of ambipolar graphene devices. With the use of nanoelectrodes, we could reduce different selected areas belonging to one single sheet as well.



INTRODUCTION

Graphene has rapidly emerged as an extremely promising system for electronic, optical, thermal, and electromechanical applications.[1] The industrial exploitation of graphene will require large-scale and cost-effective production methods, while providing a balance between ease of fabrication and final material quality. Currently, however, the preparation of graphene typically requires vacuum conditions, high temperatures, or the use of hazardous solvents.[2] Alongside physical exfoliation with scotch tape,[1b] and epitaxial methods,[3] a leading approach to graphene production is to dissociate the layers of graphite through oxidation.[4] The resulting oxygen-defect-rich graphene, known as graphene-oxide (GO), is both soluble in water and easily chemically modified[5] by chemisorption or physisorption of functional moieties. Following deposition on a surface by dip-, spin-, or spray-coating,[4f,6] π-conjugation and, consequently, electrical conductivity can be restored to a great extent by chemical reduction of GO into reduced graphene oxide (RGO), allowing to prepare graphene-based Field Effect Transistors (FETs) with graphene being either the active layer[7] or covering the source-drain electrodes.[8] The device's performance is comparable to devices based on organic polymers and gold electrodes. GO reduction is normally achieved by a thermal,[4d,e,9] chemical,[4b−d] or electrochemical[4f,10] process. The electrochemical reduction of graphene oxide to graphene is especially attractive since it is not invasive and does not require large amounts of energy, as does thermal treatment where temperatures in excess of 500 °C are used, and does not involve toxic reagents, such as hydrazine, which is often employed for chemical reduction. Previous studies described the reduction process on a macroscopic scale[4f] and in solution,[11,12] and required, for incorporation into working devices, the use of patterning steps of the graphene layer before[9] or after[10,4c,8] graphene preparation.

Recently, we have demonstrated that it is possible to obtain graphene FETs by locally patterning electrically conductive RGO regions in an insulating GO film by applying a potential between the tip of a conductive atomic force microscope (C-AFM) and a counter-electrode on the substrate surface.[13] The process relied on a water meniscus which forms around the AFM tip under ambient conditions, and acts as a localized electrochemical cell when a voltage is applied between tip and sample. The process could be performed under normal ambient conditions but, being based on the mechanical motion of a scanning probe, is inherently slow for patterning large areas, and thus hardly applicable for large-scale production of graphene.

In the present paper, we show a versatile approach for controlling the adsorption of GO at surfaces and electrochemically reducing the GO *in situ*. In particular, by choosing the right solvent, deposition, and electro-reduction conditions, we demonstrate that GO can be reduced either within a transistor channel, to serve as the semiconducting active material, or on top of one or both of the source-drain Au electrodes, in order to modify their work function by hundreds of millivolts. Thus, our all-solution based procedure enables the positioning and reduction of conductive graphene films or single sheets either on or in-between electrodes; furthermore, this is achieved in a faster and more controllable way than previously demonstrated with organic coatings.[14] We used commercially available and in-house-fabricated substrates consisting of patterned gold electrodes on

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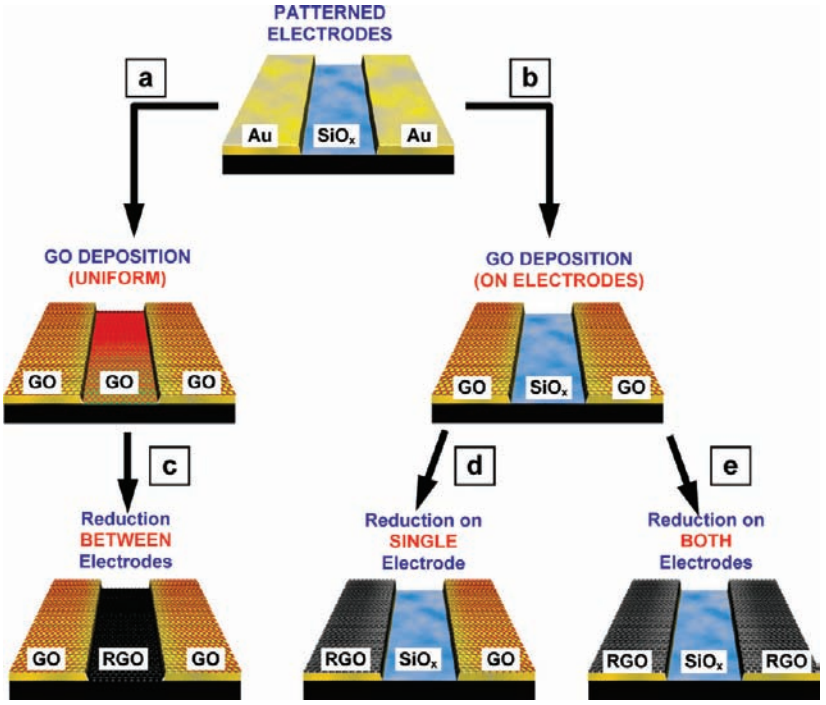

Figure 1. Schematic representation of the different FET architectures which could be achieved by selective deposition and electrochemical reduction of graphene oxide.

thermally grown silicon dioxide as the dielectric; no further lithographic or patterning steps were needed.

While previous work efficiently characterized reduction processes by spectroscopic measurement on the macroscopic scale (Raman,[7,11] IR spectroscopy,[12] voltammetry[4f,11,12]), here we follow reduction on the nanoscopic scale by using a combination of scanning probe microscopy techniques such as atomic force microscopy (AFM), Kelvin probe force microscopy (KPFM), and conductive-AFM. In this way, we monitor the evolution of the electro-reduction process with unprecedented spatial detail, in few-layer thick graphene films, single sheets, and single sheets having selectively reduced regions. This approach is simple, cheap, and technologically relevant for the incorporation of graphene into practical working electronic devices; moreover, it compares favorably with macroscopic reduction/microscopic patterning methodologies employed so far.

RESULTS AND DISCUSSION

Nonselective GO Deposition on Electrodes and Channel of FET Substrates. The configuration used for GO reduction and transistor measurements is shown in Figure 1. A bottom-contact bottom-gate configuration was employed. Silicon exposing a 200 or 230 nm thick layer of thermally grown silicon-oxide was used as a substrate (see Supporting Information). Gold source and drain electrodes with different interelectrode spacings L were produced by electron-beam lithography (L = 500 nm) and optical lithography (L ranging from 1.6 to 20 μm).

The GO is prepared by a modified Hummers method described elsewhere.[6] To obtain a uniform deposition on electrodes and gate (Figure 1a), GO in water (conc. = 5 mg/mL) was spin-coated onto the patterned substrates with a film thickness of 3 $\pm$ 1 nm, as determined by AFM measurements. More dilute GO solutions were also utilized to obtain single sheets in between the electrodes rather than continuous films.

With the exception of the transistor characterization, which was performed in an inert glovebox environment, all device preparation and testing were carried out at room temperature, with a relative humidity (RH) of 60−75%.

Selective GO Deposition on Source-Drain Electrodes. In a parallel approach (Figure 1b), GO could be deposited selectively only on the metallic electrodes, by using GO solutions in dimethylformamide (DMF) instead of water. Because of the lower polarity of DMF (polarity index (p.i.) 6.4) as compared to water (p.i. 10.2), solvent evaporation and dewetting[15] induced the selective adsorption of GO sheets on the gold electrode surfaces. The graphene was proven not to adsorb in the channel, as demonstrated by AFM measurements and by lack of macroscopic charge conduction across the electrodes even after reduction (i.e., the measured channel resistivity amounts to about 50 GΩ/μm).

Selective Reduction of GO between the Electrodes. To reduce the GO between the source-drain electrodes, a voltage was applied to the substrates having a uniform GO coating (Figure 1c). By applying source-drain voltages (ΔV) above 4 V, an irreversible increase in the conductivity of the GO in the channel was observed. A voltage of 6 V was typically applied to the drain, with a pulse duration in the range of 1−60 s. The progress of the GO reduction was monitored by performing a current−voltage measurement at low voltages (i.e., below 1 V) after each voltage pulse.

The reduction process is effective for a wide range of tested interelectrode gap sizes, ranging from 500 nm to 20 μm, and works on either continuous GO layers or single, isolated sheets. Figure 2a shows the typical increase in drain current, I_D, observed for L = 500 nm as the reduction progresses; overall, a 5 to 6 order of magnitude increase in current is observed. By applying the

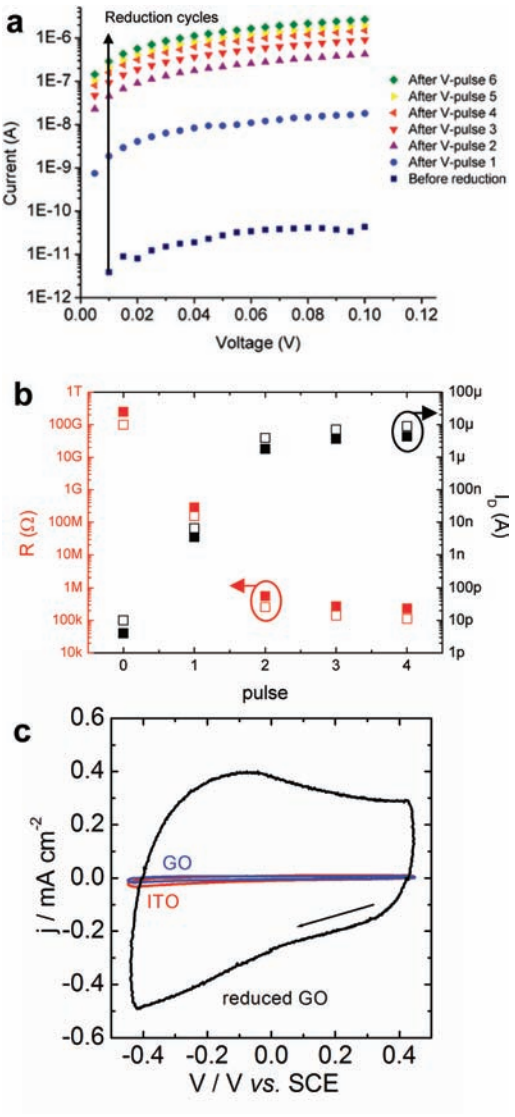

Figure 2. Voltage-induced reduction of GO, resulting in a 5 to 6 order of magnitude increase in source-drain current. (a) Source-drain current is recorded at low voltages (0−0.1 V) following each of a series of 6 V pulses. After each 6 V pulse, the current increases as a result of the voltage-induced reduction of the GO. (b) Evolution of drain current (black) and related device resistance (red) upon application of the same series of voltage pulses, as measured for 5 μm (filled squares) and 10 μm (open squares) interdigitated electrodes. (c) Cyclic voltammetry of a macroscopic sample of ITO, GO on ITO, and reduced GO on ITO at 0.5 V s^{-1} in water 0.1 mol L^{-1} KCl.

same procedure under ambient conditions, a similar increase in current has been observed on interdigitated electrodes having various width-to-length ratios (W/L between 500 and 4000). Figure 2b shows a 6 orders of magnitude increase of the current I_D (black data-points) achieved for electrodes with L = 5 μm (filled) and L = 10 μm (open) after four successive 60 s voltage pulses of 6 V. I_D values are measured by applying V_D = 1 V for 1 s. In all cases, both in the reduction procedure as well as in the I_D measurement, the gate electrode is grounded.

The measured sheet resistance amounts to 180 ± 130 KΩ/sq. This value is obtained by taking into account the contact resistance contribution estimated from measurements at different channel lengths spanning from 2.5 to 20 μm (the so-called transfer line method, see Supporting Information).

A wide range of applied potential voltages was studied. Overall, no effect is observed at low voltages (ΔV < 3 V), even for long processing times (i.e., 10 h), while for an applied potential between 4 and 6 V, we observe an increase of the GO reduction after each pulse (as shown in Figure 2). By applying ΔV = 7 V, some of the samples (about 50%) show an abrupt increase in the source-drain resistance, in the gigaohm (GΩ) range, indicative of material damage. This may be explained by a strong mechanical stress due to gas formation during the electrolysis of the water layer adsorbed at the GO/electrode interface where the electric field is higher. Thus, the reduction procedure was generally performed by applying ΔV = 6 V, corresponding to the highest potential value that can be employed without damaging the material.

In all cases, the electro-reduction process is complete after less than 10 cycles. The number of cycles needed to achieve saturation is independent of the channel length within the tested range of 500 nm to 20 μm, whereas it is dependent on the applied potential: the larger the potential, the smaller the number of cycles required for saturation. When a 6 V potential is applied, saturation is achieved after 7−8 cycles of 60 s voltage pulses.

Nanoscopic Characterization of the Reduction Process. The reduction process was studied by means of high-resolution SPM techniques in few-layer thick GO films and at the single sheet level. Kelvin Probe Force Microscopy (KPFM) and conductive AFM (C-AFM) techniques enabled the mapping of the surface potential and the conductivity between the source-drain electrodes, respectively.

KPFM is a contact-less technique, which can quantitatively map the electrical potential of nanostructured samples with a lateral resolution of about 20 nm, and a potential resolution of a few millivolts, with minimal perturbation of the sample.[16] For these reasons, it has been widely used to measure charge generation and transport in transistors and photovoltaic blends,[16a,17] and to characterize the electrical properties of GO and RGO mono- and multilayers (for a more detailed description of KPFM applications to the study of graphene, see ref 7). Here, we used KPFM to monitor both the change in surface potential of the reduced graphene sheets, and the potential decay in the channel region of a working FET. The effect of electro-reduction on sample properties was studied both on continuous GO films with about 3 nm thickness and in less dense coatings, where single sheet reduction could be observed.

Figure 3 displays the topography gradient (a) and the corresponding potential map (b) for a continuous GO layer covering source-drain interdigitated electrodes with a 2 μm gap (see Supporting Information). The potential map $\Delta V(x,y)$, corresponding to the local voltage, is obtained by subtracting the KPFM image acquired with polarized drain and grounded source with the one acquired on the same area with both grounded electrodes: $\Delta V(x,y) = SP|_{V_D=1} - SP|_{V_D=0}$.[18] The topography gradient is shown instead of the usual topography, to visualize both the boundaries of the thin GO sheets and the thick electrodes. A source drain-voltage of 1 V was applied during the measurement in order to map the potential decay across the electrode gap.

Unlike KPFM, in Conductive-AFM (C-AFM), the tip is in physical contact with the sample. A bias is applied to the sample while the tip is grounded, and the resulting current is measured. In Figure 4, a topographic AFM image (a) and the corresponding C-AFM current map (b) of the system are shown. For the sake of

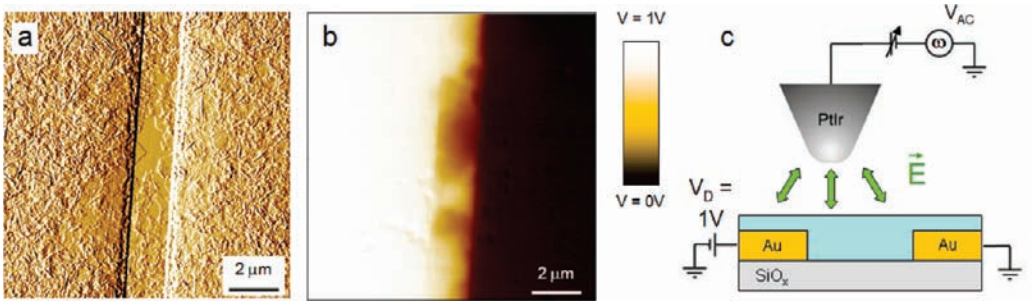

Figure 3. KPFM mapping of surface potential in a FET based on voltage-reduced GO. (a) AFM topography gradient image and (b) corresponding potential map acquired by applying a 1 V potential voltage to the left electrode while the right one is grounded. (c) Schematic representation of KPFM measurement. *Z*-ranges: (a) 100 nm/μm and (b) 1 V.

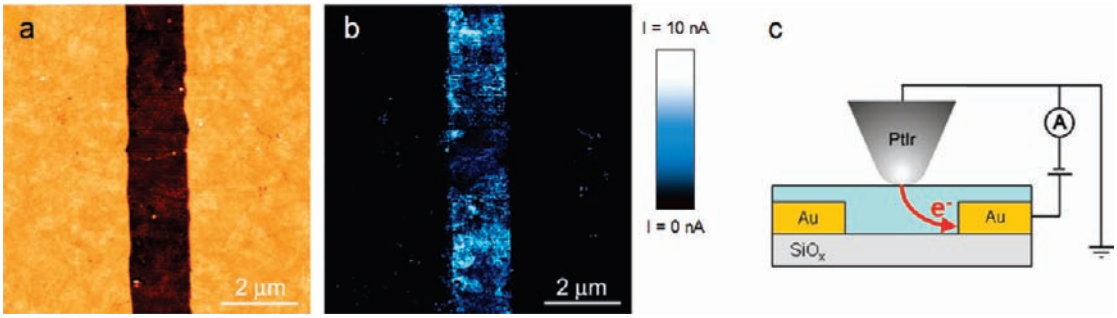

Figure 4. C-AFM current mapping of voltage-reduced GO in an FET channel. Simultaneously recorded (a) AFM topography and (b) current image of voltage-reduced GO between (unreduced) GO-covered Au electrodes. (c) Schematic representation of the C-AFM measurement (both Au electrodes are electrically connected; this is omitted in the diagram for simplicity). *Z*-ranges: (a) 50 nm and (b) 10 nA.

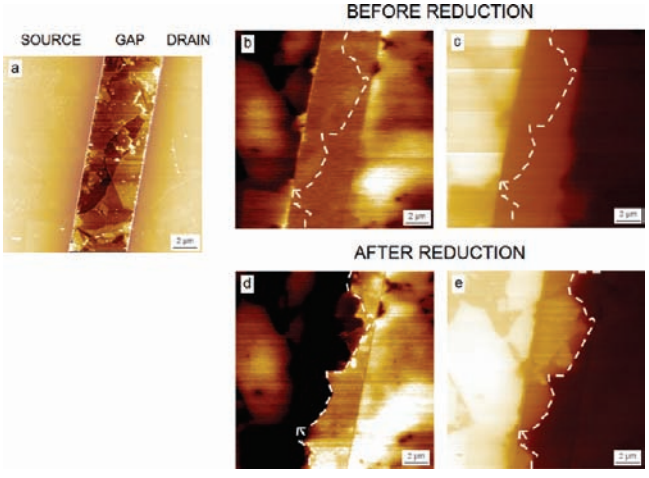

Figure 5. Electro-reduction between source-drain electrodes. Samples with a low GO coverage are shown, to demonstrate reduction of single sheets. (a) AFM topography image of an FET substrate with the gap partially covered by single sheets of GO. Some sheet edges in the channel have been outlined by a white dotted line. (b and c) Corresponding potential image obtained by KPFM, with both electrodes grounded (b) or with a 1 V bias applied between source and drain (c) showing no potential decay across the channel. (d and e) Same as panels b and c, but after selective electroreduction of the electrode on the right. Under bias (e), the sheets in the channel follow the bias of the right electrode to which they are connected. Z ranges: (a) 80 nm (8 nm in the gap), (b and d) 100 mV, and (c and e) 800 mV.

simplicity, the gate electrode is not included in Figures 3 and 4. The GO-covered electrodes exhibit no current (within the limits of the C-AFM resolution) for the bias that was used (100 mV), with only some nanoscopic pinholes in the film passing current. However, between the electrodes, the film has become highly conductive, due to the voltage-induced reduction of the GO. The change in current before and after the reduction, measured by C-AFM, is consistent with source-drain current measurements, with an increase of at least 4 orders of magnitude, from below the detection limit of the instrument (<1pA) to nearly 10 nA over the most conductive regions.

Figure 5 shows how changes due to the electro-reduction process could be detected by KPFM even at single sheet level. In this case, a low coverage of GO has been used, to better discriminate single sheets and the details of the process. AFM topography (Figure 5a) displays several single GO sheets deposited in the gap between the electrodes. The sheets are insulating, and have a similar potential to the underlying silicon oxide substrate, as visualized by KPFM (Figure 5b). If a small potential difference is applied between the electrodes (Figure 5c), the two electrodes vary their potential, but no change is observed in the gap. After the electrochemical reduction, instead, the sheets connected to the right electrode become visible by KPFM (Figure 5d). Upon biasing the electrodes, the sheet potential now follows that of the electrodes, thus providing clear evidence for the change in GO conductivity (Figure 5e). It is worth noting that the electro-reduction process has an influence even on the sheet morphology, inducing in some cases a slight up-folding of the sheet edges, as visualized by AFM (see Figure S3 in Supporting Information).

Asymmetric Reduction of GO on the Electrodes. GO reduction was performed on sheets selectively deposited on the gold electrodes by dip coating in DMF (Figure 1b, previously

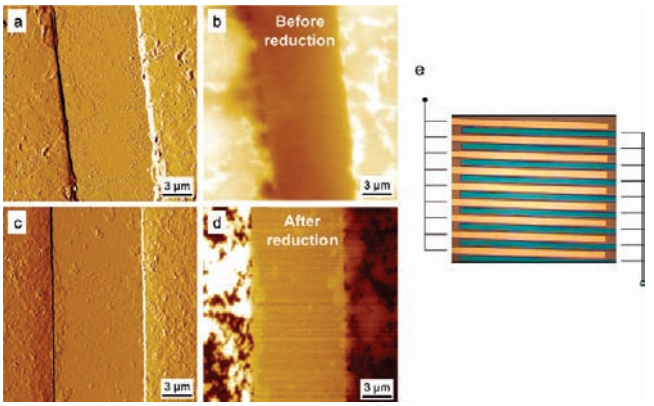

Figure 6. (a and c) Gradient filtered AFM topography and (b and d) corresponding potential images of GO sheets selectively deposited on drain-source electrodes before (a and b) and after (c and d) selective reduction of the sheets on the right electrode. (e) Macroscopic deposition of GO on selected electrodes, as visible by optical microscopy. Uncoated gold electrodes appear yellow, coated ones are blue. See Supporting Information for more details. *Z*-range = (a and c) 100 nm/μm, (b and d) 160 mV.

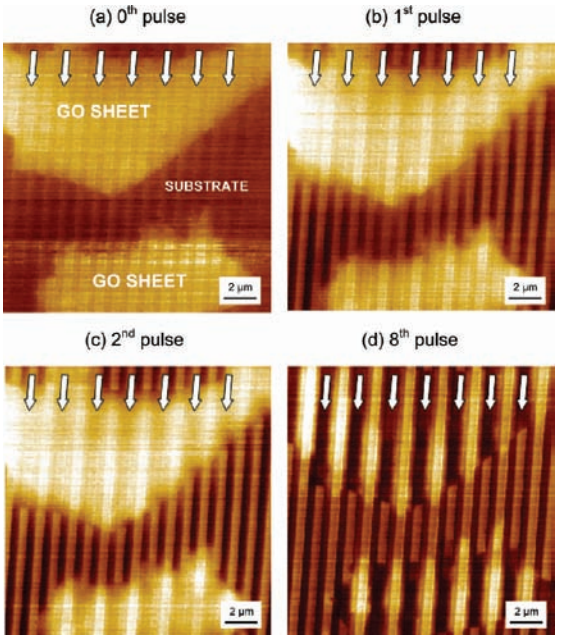

Figure 7. Selective reduction on single GO sheets on interdigitated nanoelectrodes, upon a series of voltage pulses at −6 V. The number in each image indicates the number of pulses; white arrows indicate the electrodes to which the voltage has been applied.

described). The reduction was accomplished by applying a voltage of 1 V for 60 min to one (Figure 1d) or both (Figure 1e) of the electrodes, while the sample was immersed in water. The potential, measured with respect to a macroscopic reference gold electrode in the water, prevents water oxidation at the anode. The electro-chemical reaction was monitored by measuring the current through the cell (i.e., micro/water/macro-reference electrode). A slow current variation was achieved and the asymptotic value, close to the pristine one, is restored after about 60 min of continuous applied potential. After the treatment, KPFM shows a clear difference between the potential of the two electrodes (Figure 6) providing evidence for the alignment of RGO sheets to the potential of the gold electrodes. The potential profile of the reduced and unreduced GO, as compared to the one of gold electrodes, is reported in Figure S4 in the Supporting Information.

Depending on the experimental conditions, the GO surface potential (SP) could be tuned from 200 mV above to 150 mV below the SP of gold, which is 350 mV lower than that of the pristine GO. The electro-reduction process goes to completion after applying 10 voltage pulses. After this, no changes in the SP are observed even after applying a steady potential overnight, or exposing the samples to ambient conditions. The evolution of SP upon treatment and an overnight stability test are reported in Figure S8 in Supporting Information. Massive deposition of GO on macroscopic electrodes could also be achieved (Figure 6e) by applying a potential directly during GO deposition, as detailed in the Supporting Information, but in this case, no single sheets could be visualized.

Selective Reduction of Different Areas of a Single GO Sheet. By using nanoelectrodes, we could achieve not only the selective reduction of different sheets, but also the selective reduction of different areas on a single sheet. Figure 7 shows the KPFM potential image of a single, well-defined GO sheet deposited on interdigitated electrodes. The electrodes have a spacing of 500 nm, while the sheets are much larger, thus, spanning several electrodes pairs. By applying a potential to the source electrode, a selective reduction of the areas close to the electrodes is achieved, which progresses with each pulse. In this case, similar to what is shown in Figure 3 but on a smaller scale, the reduction process spreads across the gap, creating conductive paths between the electrodes. The final result is a graphene sheet having parallel, alternating stripes of oxidized (insulating) and reduced (conductive) areas.

By using the right voltage and nanoscale electrodes, the process could in theory be scaled down further, to create "striped" graphene, with conductive ribbons in an otherwise-insulating GO sheet.

Current−voltage Characterization of RGO-Based FETs. The charge transport properties of the electrochemically reduced RGO were studied by FET characterization, using the same electrodes as the electro-reduction. The stability of the reduction process for FETs working over long times was also tested.

A voltage was applied between source and drain (V_{sd}), and the current was measured at the drain electrode (I_D) while varying the Si back-gate potential. A distinct ambipolar transport behavior, typical of graphene and RGO, was observed. An average electron mobility of 0.05 ± 0.01 $cm^2/(V\,s)$ and hole mobility of 0.12 ± 0.01 $cm^2/(V\,s)$ were extracted, based on several FET devices, from the transfer curves in the linear regime (Figure 8). These values approach the mobilities detected by C-AFM tip-reduced GO (0.1 $cm^2/(V\,s)$ and 0.3 $cm^2/(V\,s)$, respectively),[13c] and are within 1 order of magnitude of the mobilities obtained for devices employing GO reduced with aggressive, macroscopic methods, that is, by combined hydrazine and thermal treatments.[19] Finally, no degradation of FET performances was observed after repeated voltage sweeps, or after storage under ambient conditions.

Cyclic Voltammetry Characterization of Reduction Process. To complement the characterization of micro-scale GO reduction in between microelectrodes, uniform thin layers of the same GO material were also studied by cyclic voltammetry (CV, see Supporting Information for experimental details). The reduction of GO films (about 50 nm thick) was clearly observed

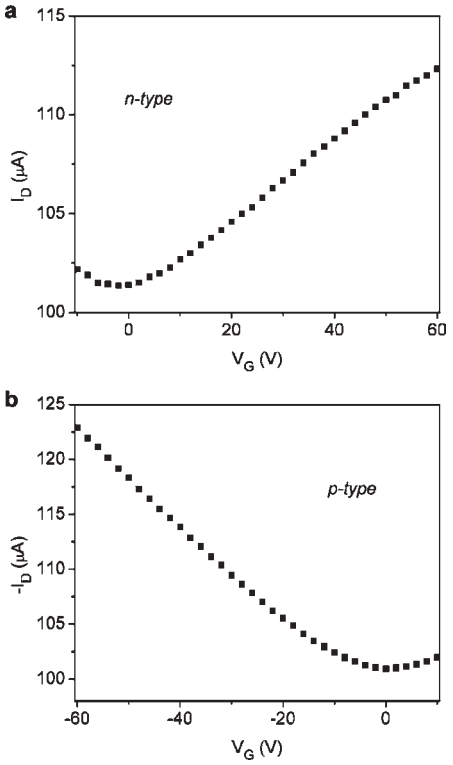

Figure 8. Voltage-reduced GO FET characteristics. Transfer curves measured on voltage-reduced GO transistors, in the (a) n-type (Vsd = +2 V), (b) p-type (V_{sd} = −2 V) transport regimes. Channel length = 1.6 μm.

through an irreversible reduction wave, with a maximum at −1.16 V versus SCE (see Supporting Information), which disappeared in further voltage sweeps. The reduction process was also visible in this case by naked eye, with the GO getting darker while transforming into RGO (Figure.S6). The RGO layer obtained in this way shows capacitive currents about 20 times higher (Figure 2c) than the clean reference substrate (conductive ITO), due to the high conductivity and surface area typical of graphene, suggesting possible applications in energy storage.[20]

By analogy with the previously studied case of C-AFM tip-induced reduction,[13c] the reduction results from an electrochemical process whereby hydrogen ions are generated through the oxidation of water.[4f] In the case of the reduction performed under ambient conditions, water is present as a thin adsorbed layer at the GO surface.

The suggested reaction scheme leading to GO reduction is hypothesized to comply with the following:

$$\mathrm{GO} + a\mathrm{H}^+ + b\mathrm{e}^- \rightarrow \mathrm{rGO} + c\mathrm{H_2O} \quad \text{(reduction of GO)} \qquad (1)$$

$$2\mathrm{H_2O} \rightarrow 4\mathrm{H}^+ + 4\mathrm{e}^- + \mathrm{O_2} \quad \text{(oxidation of water)} \qquad (2)$$

Considering from CV a reduction potential of −1.16 V versus SCE (−0.92 vs SHE) and a standard potential of +1.23 V for (2), a cell potential of ca. 2.15 V can be determined for the whole redox reaction, being much smaller than the one experimentally used to accomplish nanoscale GO reduction (3.6 V).[13c] This observation suggests that other parameters, such as a voltage drop (due to series resistance at the graphene−water and gold−graphene interfaces), pH, and oxygen concentration, should be taken into account.

Upon reduction, the graphene coated surface becomes less hydrophilic with respect to the pristine GO, as evidenced by a change in contact angle values from 73° to 85°. This can be ascribed to the loss of carboxyl and hydroxyl groups. The reduction of a thick GO film on ITO was also monitored by measuring the ionization energy (IE) of the two samples with photoelectron spectroscopy (AC-2; RKI Instruments). IE represents the energy difference between the vacuum level and the binding energy of the top valence band (HOMO in a molecular representation). We observe a decrease of the IE upon the reduction from 5.30 ± 0.02 to 4.87 ± 0.02 eV, in agreement with ref 21. This can be attributed to the higher energy gap in an insulating material as GO if compared to a more conductive one like RGO.

CONCLUSIONS

In summary, we described a highly versatile method that relies on a voltage applied between the source and drain electrodes of a transistor to trigger the electrochemical reduction of graphene oxide by using a thin layer of adsorbed water as electrolyte.

Our modular approach to the reduction process can be tuned by:

1. Exploiting solvent dewetting to predeposit GO either uniformly on the substrate, or only on the metallic electrodes.
2. Varying the amount and type of solvent used during the electro-reduction (thin water layer from environmental humidity, or dipping the sample in water or DMF).
3. Changing the geometry of the system (using macro-micro electrodes and varying the electrode spacing).

When the whole sample is immersed in solution and a potential is applied between the drain and an external, macroscopic electrode, current will flow through the whole metal-solution interface, and thus uniform reduction on the whole electrode will take place, while no current will flow between source and drain electrodes. Conversely, when only a thin layer of water is present on the sample, the current will flow mostly between the source and drain electrodes, thus reducing the GO present in the gap and forming an active region. In this case, the channel length is much larger ($L > 2$ μm) than the thickness of water layer on the surface (few nm). We can consider the lines of the electric field between the two electrodes to be parallel to the substrate surface, and the sample can be approximated as a two-dimensional system. All the boundaries effects can be neglected and no reduction is achieved on GO on top the electrodes even if water coats all the surface of the sample. Instead, in the case of submicrometer (i.e., 500 nm) channel lengths, the boundary effects cannot be neglected. The distribution of the electric field is more complex (a 3D picture) and also the electrode edges are more involved into the reduction processes. Through the water, the current passes not only along the gap, but throughout the electrode surface, causing GO reduction in a region close to the polarized electrode (see Figure 7).

The possibility to use the prepatterned source-drain electrodes to build the active layer in between the electrodes with the present self-aligned process is much simpler and faster than postdeposition patterning. While the study of the reduction process was limited here to a scale of tens of nanometers due to the electrode size and the resolution of scanning probe techniques, increasingly localized

electro-reduction could be in principle achieved on a smaller (nano) scale by using highly localized electric fields.

Our approach is simple and quick, making it possible to engineer reduced graphene oxide devices and circuits in a few minutes. The voltage-induced reduction process works under ambient conditions, with different channel lengths, and FET geometries. It has been successfully used for the selective reduction of either single sheets or continuous layers, and does not require specialized equipment. We anticipate that it can be applied in parallel on a wide variety of substrates, making the process attractive for large-scale, low-cost processing.

■ ASSOCIATED CONTENT

Supporting Information. Further details about the experimental methods, process of GO reduction, and potential mapping. This material is available free of charge via the Internet at http://pubs.acs.org.

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